九齊科技股份有限公司
Nyquest Technology Co., Ltd.

DATA SHEET

NY5P Series *(OTP for NY5)*

Single-Chip 4-bit MCU with 15~24 I/O and 4-Ch Speech/Midi

Version 1.6

Jun. 06, 2013

Revision History

Version	Date	Description	Modified Page
1.0	2010/12/10	Formal release.	-
1.1	2010/12/11	1. The OSC pad is set as PD2 when NY5A uses external OSC pad. 2. External OSC pad “PD2/OSC” is connected to V_{REG} pad.	5 11
1.2	2011/01/05	1. Add Chinese description for Chapter 1 & 2. 2. External OSC pad “PX#/OSC” is connected to V_{REG} pad.	3, 4, 5 11, 15
1.3	2011/10/24	1. Add NY5P185A, NY5P345A, NY5P520A application circuit. 2. Add NY5P185A, NY5P345A, NY5P520A die pad diagram. 3. Add NY5P185A, NY5P345A, NY5P520A COB pin assignment. 4. Add NY5P185A, NY5P345A, NY5P520A package information. 5. Modify COB PCB size.	16, 17 18, 19 19, 20 20, 22 23
1.4	2012/03/23	1. Add NY5P345A, NY5P520A 64-pin LQFP package information.	21, 24, 25
1.5	2012/10/31	1. NY5P supports all new NY5AxxxB, NY5BxxxB & NY5CxxxB. 2. Add 2MHz instruction frequency. 3. Modify OSC vs VDD curve. 4. Add new package type NY5P345AS28 (28-pin SOP). 5. Add new package type NY5P520AS28 (28-pin SOP).	3, 4, 6, 7 4, 7, 13 14 21, 26 21, 26
1.6	2013/06/06	1. Add NY5P720A new body and related information.	3, 6, 17, 19, 22, 20, 26

1. 概述

NY5P系列產品爲多功能單晶片CMOS語音合成4位元微控制器，是九齊科技爲了支援 NY5A, NY5B, NY5C 系列 MaskROM 產品所專門開發的崁入式EPROM架構的OTP IC (One Time Programmable)。提供4通道的語音/Midi合成功能，語音合成方式採用先進的高音質ADPCM演算法，最高採樣率可達CD音質44.1kHz，且硬體有16階的音量控制。提供兩種聲音輸出方式可供選擇，一種PWM輸出和一種DAC輸出。使用RISC精簡指令集架構，共有48條指令，除了少數指令需要2個時序，大多數指令都是1個時序即可完成，可以很方便的以程式控制來完成不同的應用。利用精準的+/-1%內阻震盪，客戶可以不需外加震盪電阻，但是彈性的預留一個OSC腳位可以外接震盪電阻，當只使用內阻震盪時，此腳可以當作一般I/O腳使用。提供待機模式(Halt mode)，可大幅度的節省功耗；另外還提供慢速模式(Slow mode)，可以降低功耗。

2. 功能

- 寬廣的工作電壓： 2.0V ~ 5.5V。*(同 MaskROM IC 的工作電壓範圍2.0V ~ 5.5V)*
- 4-bit RISC 精簡指令集架構的微控制器，共有48條指令。
- 共有7個OTP母體，最大母體的ROM容量爲1728Kx10-bit，程式和資料共用同一塊ROM。ROM容量，秒數和I/O腳數如下：

產品編號 (OTP)	語音長度 (秒) @6kHz	ROM 容量 (10-bit)	I/O 腳數
NY5P025A	25.0	64k x 10	15 (PA, PB, PC, PD0~2)
NY5P055A	55.0	136k x 10	15 (PA, PB, PC, PD0~2)
NY5P085A	85.0	208k x 10	15 (PA, PB, PC, PD0~2)
NY5P185A	185.0	448k x 10	20 (PA, PB, PC, PD, PE)
NY5P345A	345.0	832k x 10	20 (PA, PB, PC, PD, PE)
NY5P520A	518.3	1248k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5P720A	718.3	1728k x 10	24 (PA, PB, PC, PD, PE, PF)

NY5A系列 MaskROM IC 的實際容量，秒數和I/O腳數如下：

產品編號 (MaskROM)	語音長度 (秒) @6kHz	ROM 容量 (10-bit)	I/O 腳數
NY5A003B	3.3	12k x 10	8 (PA, PB)
NY5A005B	5.0	16k x 10	8 (PA, PB)
NY5A008B	8.3	24k x 10	8 (PA, PB)
NY5A011B	11.7	32k x 10	8 (PA, PB)
NY5A018B	18.3	48k x 10	8 (PA, PB)
NY5A025B	25.0	64k x 10	8 (PA, PB)
NY5A035B	35.0	88k x 10	8 (PA, PB)
NY5A045B	45.0	112k x 10	8 (PA, PB)
NY5A055B	55.0	136k x 10	8 (PA, PB)
NY5A065B	65.0	160k x 10	8 (PA, PB)

NY5B系列 MaskROM IC 的實際容量，秒數和I/O腳數如下：

產品編號 (MaskROM)	語音長度 (秒) @6kHz	ROM 容量 (10-bit)	I/O 腳數
NY5B005B	5.0	16k x 10	15 (PA, PB, PC, PD0~2)
NY5B008B	8.3	24k x 10	15 (PA, PB, PC, PD0~2)
NY5B011B	11.7	32k x 10	15 (PA, PB, PC, PD0~2)
NY5B018B	18.3	48k x 10	15 (PA, PB, PC, PD0~2)
NY5B025B	25.0	64k x 10	15 (PA, PB, PC, PD0~2)
NY5B035B	35.0	88k x 10	15 (PA, PB, PC, PD0~2)
NY5B045B	45.0	112k x 10	15 (PA, PB, PC, PD0~2)
NY5B055B	55.0	136k x 10	15 (PA, PB, PC, PD0~2)
NY5B065B	65.0	160k x 10	15 (PA, PB, PC, PD0~2)
NY5B075B	75.0	184k x 10	15 (PA, PB, PC, PD0~2)
NY5B085B	85.0	208k x 10	15 (PA, PB, PC, PD0~2)

NY5C系列 MaskROM IC 的實際容量，秒數和I/O腳數如下：

產品編號 (MaskROM)	語音長度 (秒) @6kHz	ROM 容量 (10-bit)	I/O 腳數
NY5C112B	111.7	272k x 10	20 (PA, PB, PC, PD, PE)
NY5C132B	131.7	320k x 10	20 (PA, PB, PC, PD, PE)
NY5C158B	158.3	384k x 10	20 (PA, PB, PC, PD, PE)
NY5C185B	185.0	448k x 10	20 (PA, PB, PC, PD, PE)
NY5C225B	225.0	544k x 10	20 (PA, PB, PC, PD, PE)
NY5C265B	265.0	640k x 10	20 (PA, PB, PC, PD, PE)
NY5C305B	305.0	736k x 10	20 (PA, PB, PC, PD, PE)
NY5C345B	345.0	832k x 10	20 (PA, PB, PC, PD, PE)
NY5C450B	451.7	1088k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C520B	518.3	1248k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C640B	638.3	1536k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C720B	718.3	1728k x 10	24 (PA, PB, PC, PD, PE, PF)

- 224x4-bit RAM，分成4頁，每頁56x4-bit。
- 1MHz 或 2MHz指令頻率。
- 提供慢速模式(Slow mode)，可降低功耗。*(注意: 由於慢速模式的時間誤差較大，不建議使用在計時的應用)*
- 提供待機模式(Halt mode)，可節省功耗，靜態電流(Isb)小於1uA。
- 精準的+/-1%內阻震盪；另外還提供外阻震盪選擇，以便調整速度。
- 提供低壓復位(LVR=1.8V)，看門狗計時(WDT)，I/O復位功能(External Reset)。
- 一個中斷輸入可連結到一組獨立的堆棧(Stack)，並有多種中斷來源可以使用。

- 15~24根彈性的I/O腳，可設定爲input, output, large current output, IO, floating-type reset, pull-high reset, IR carrier output 和 large current IR carrier output 等輸入輸出功能。當做爲輸出時，可以選擇爲一般輸出電流(Normal Drive Current, Normal Sink Current) 或是大電流輸出(Large Sink Current)，可直推高亮度LED，不需外加三級管。
- 支援Open-Drain (OD) 的雙向I/O。
- IR紅外線輸出: 提供31kHz~58kHz可選擇的紅外線頻率輸出，並可選擇高電平/低電平編碼。
- 提供4通道的語音/Midi合成功能，可以單獨設定每個通道爲語音或Midi輸出。
- 更先進的高音質ADPCM語音合成演算法，可以經由簡單的調整採樣位數來提升音質。
- 提供256點, ADSR 和 Full-Wave 3種音色合成方法，用於進行不同Midi音色的編輯。
- 內建256階Midi包絡線控制(Envelope Control)，用於進行Midi音量的控制。
- 一組9-bit PWM純硬體輸出，可以直接驅動喇叭或蜂鳴片；一組10-bit DAC純硬體輸出，可以外加放大線路來放大音量 (通常用於多通道輸出)。
- 提供大音量PWM輸出，可以直接輸出更大音量，輸出語音不需外加三級管放大。
- 內建16階硬體音量控制(Volume Control)，用於進行整體音量的控制。
- 支援 Quick-IO 訊號控制。
- 提供特殊的快速燒錄模式，以加快OTP燒錄時間。
- 支援特殊的ICP (In Circuit Programming) 燒錄功能，以方便客戶先組裝PCBA模組再進行燒錄。
- 提供可程式的Code資料保護模式。*(當Security-Bit 被燒斷後，資料將無法讀取。)*
- 提供多種出貨型態，以滿足客戶不同的應用需求。

(要進一步瞭解上述功能，請參考NY5A, NY5B, NY5C 的規格書，或聯繫九齊科技或九齊代理商。)

1. GENERAL DESCRIPTION

The NY5P series IC is a powerful 4-bit micro-controller based sound processor. They are embedded EPROM architecture, and the OTP (One Time Programmable) ICs that are designed to support NY5A, NY5B and NY5C MaskROM products. There are 4 channels that are configured as speech or midi, and all of them can be auto-played back simultaneously. By using the high fidelity ADPCM speech synthesis algorithm, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz and different volume level are supported. It is also equipped two kinds of audio outputs with fine resolution, including a current D/A converter and a PWM direct-drive. The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 48 instructions, and most of them are executed in single cycle. Through +/-1% accurate internal oscillation, external Rosc is mostly unnecessary. Also an OSC pad is reserved for external oscillation, and this pad can be optioned as normal I/O when setting internal oscillation only. Furthermore, in addition to the HALT mode (sleep mode), it offers the SLOW mode to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 2.0V to 5.5V. *(Same as MaskROM products)*
- 4-bit RISC type micro-controller with 48 instructions.
- There are 7 OTP bodies. 1728Kx10-bit ROM is the maximum. Program and voice data share the same ROM space. The voice duration, ROM size and I/O counts are shown below.

Product (OTP)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
NY5P025A	25.0	64k x 10	15 (PA, PB, PC, PD0~2)
NY5P055A	55.0	136k x 10	15 (PA, PB, PC, PD0~2)
NY5P085A	85.0	208k x 10	15 (PA, PB, PC, PD0~2)
NY5P185A	185.0	448k x 10	20 (PA, PB, PC, PD, PE)
NY5P345A	345.0	832k x 10	20 (PA, PB, PC, PD, PE)
NY5P520A	518.3	1248k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5P720A	718.3	1728k x 10	24 (PA, PB, PC, PD, PE, PF)

Regarding NY5A MaskROM series, the voice duration, ROM size and I/O counts are shown below.

Product (MaskROM)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
NY5A003B	3.3	12k x 10	8 (PA, PB)
NY5A005B	5.0	16k x 10	8 (PA, PB)
NY5A008B	8.3	24k x 10	8 (PA, PB)
NY5A011B	11.7	32k x 10	8 (PA, PB)
NY5A018B	18.3	48k x 10	8 (PA, PB)
NY5A025B	25.0	64k x 10	8 (PA, PB)

NY5A035B	35.0	88k x 10	8 (PA, PB)
NY5A045B	45.0	112k x 10	8 (PA, PB)
NY5A055B	55.0	136k x 10	8 (PA, PB)
NY5A065B	65.0	160k x 10	8 (PA, PB)

Regarding NY5B MaskROM series, the voice duration, ROM size and I/O counts are shown below.

Product (MaskROM)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
NY5B005B	5.0	16k x 10	15 (PA, PB, PC, PD0~2)
NY5B008B	8.3	24k x 10	15 (PA, PB, PC, PD0~2)
NY5B011B	11.7	32k x 10	15 (PA, PB, PC, PD0~2)
NY5B018B	18.3	48k x 10	15 (PA, PB, PC, PD0~2)
NY5B025B	25.0	64k x 10	15 (PA, PB, PC, PD0~2)
NY5B035B	35.0	88k x 10	15 (PA, PB, PC, PD0~2)
NY5B045B	45.0	112k x 10	15 (PA, PB, PC, PD0~2)
NY5B055B	55.0	136k x 10	15 (PA, PB, PC, PD0~2)
NY5B065B	65.0	160k x 10	15 (PA, PB, PC, PD0~2)
NY5B075B	75.0	184k x 10	15 (PA, PB, PC, PD0~2)
NY5B085B	85.0	208k x 10	15 (PA, PB, PC, PD0~2)

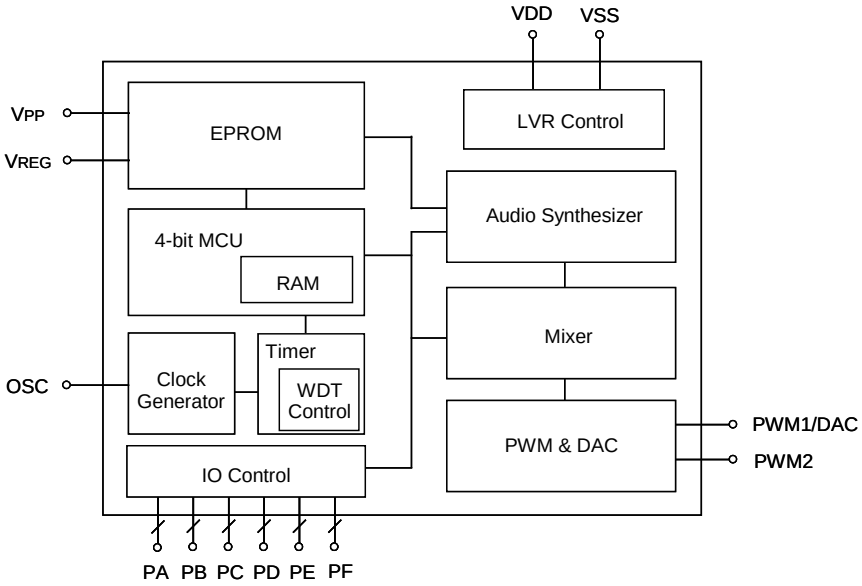
Regarding NY5C MaskROM series, the voice duration, ROM size and I/O counts are shown below.

Product (MaskROM)	Voice Duration (sec) @6kHz	ROM Size (10-bit)	I/O
NY5C112B	111.7	272k x 10	20 (PA, PB, PC, PD, PE)
NY5C132B	131.7	320k x 10	20 (PA, PB, PC, PD, PE)
NY5C158B	158.3	384k x 10	20 (PA, PB, PC, PD, PE)
NY5C185B	185.0	448k x 10	20 (PA, PB, PC, PD, PE)
NY5C225B	225.0	544k x 10	20 (PA, PB, PC, PD, PE)
NY5C265B	265.0	640k x 10	20 (PA, PB, PC, PD, PE)
NY5C305B	305.0	736k x 10	20 (PA, PB, PC, PD, PE)
NY5C345B	345.0	832k x 10	20 (PA, PB, PC, PD, PE)
NY5C450B	451.7	1088k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C520B	518.3	1248k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C640B	638.3	1536k x 10	24 (PA, PB, PC, PD, PE, PF)
NY5C720B	718.3	1728k x 10	24 (PA, PB, PC, PD, PE, PF)

- 224x4-bit RAM maximum, divided into 4 pages.
- 1MHz or 2MHz instruction frequency.
- SLOW mode to operate at low power consumption. *(Not suggest using in Timer/Clock application.)*

- HALT mode to save power, less than 1uA@3V standby current.
- Precisely embedded oscillator with build-in resistor (+/- 1%). External resistor to adjust system frequency is optional.
- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.
- One interrupt entrance with an independent stack, multiple interrupt sources.
- Maximum 24 flexible I/Os maximum with optional function: input, output, large current output, IO, floating-type reset, pull-high reset, IR carrier output and large current IR carrier output. For the output port, users can select the normal Drive current output or large Sink current output to directly drive high brightness LED.
- Support Open-Drain (OD) bi-direction IO.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- Maximum of 4 channels can play simultaneously; each channel can be arbitrarily assigned as speech or Midi channel based on the product spec.
- New high fidelity ADPCM speech synthesis algorithm.
- 3 kinds of 256 points, ADSR and Full-Wave instrument waveform provide outstanding midi quality for MIDI.
- 256 steps envelope control for Midi.
- High quality 9-bit PWM to directly drive speaker, or 10-bit D/A converter audio output to amplify the volume by external audio amplifier for multi-channel MIDI especially.
- Support large PWM current output.
- 16 steps volume control for audio output.
- Quick-IO control supported.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP *(In Circuit Programming)* writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*
- Various shipping type for different application requirement.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

Pad Name	ATTR.	Description
Vpp	Power	Positive high power for programming.
V_{REG}	Power	Regulator input. Connect a 0.1uF cap to GND or keep floating.
VDD#	Power	Positive power.
GND#	Power	Negative power.
PA0/SDA	I/O	Bit 0 for Port A, or serial data input at programming mode.
PA1/SCL	I/O	Bit 1 for Port A, or serial clock input at programming mode.
PA2~3	I/O	Bit 2~3 for Port A.
PB0~3	I/O	Bit 0~3 for Port B.
PC0~3	I/O	Bit 0~3 for Port C.
PD0~1	I/O	Bit 0~1 for Port D.
PD2/OSC	I/O	Bit 2 for Port D, or External resistor for oscillator input.
PD3	I/O	Bit 3 for Port D. *(PD3 for NY5P185A, NY5P345A, NY5P520A & NY5P720A.)*
PE0~2	I/O	Bit 0~2 for Port E. *(PE0~3 for NY5P185A, NY5P345 A, NY5P520A & NY5P720A.)*
PE3/OSC	I/O	Bit 3 for Port E, or External resistor for oscillator input.
PF0~2	I/O	Bit 0~2 for Port F. *(PF0~3 for NY5P520A & NY5P720A.)*
PF3/OSC	I/O	Bit 3 for Port F, or External resistor for oscillator input.
PWM1/DAC	O	PWM1 output or DAC output.
PWM2/Mode	O	PWM2 output, or select programming mode.

* NY5P025A, NY5P055A, NY5P085A: OSC pad is shared with PD2.

* NY5P185A, NY5P345A: OSC pad is shared with PE3.

* NY5P520A, NY5P720A: OSC pad is shared with PF3.

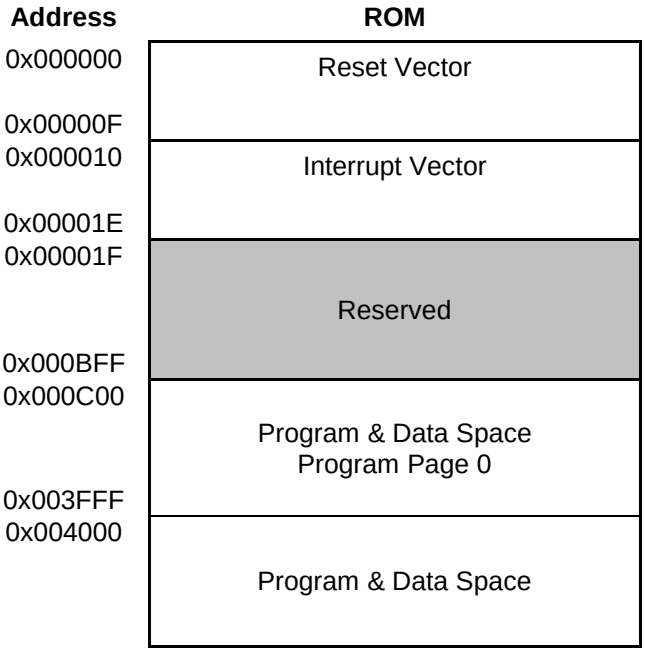
* When NY5A uses external OSC pad of PB3/OSC, the OSC pad for NY5P025A, NY5P055A and NY5P085A is set as PD2.

5. MEMORY ORGANIZATION

There are maximum 1728K words EPROM, 224 nibbles of RAM and 19 nibbles of dedicated system control register. The registers are divided into 11 nibbles of system registers and 8 nibbles of memory registers. Besides, there are several registers without address allocation, and they can only be accessed by the special instructions. One of the registers is RAM page register (PG), and the others are audio control registers.

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 14-bit length address of ROM, the program page size is 16K words.



5.2 RAM

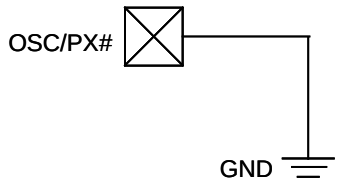
Each page of RAM contains 56 nibbles, and NY5P serial provides 224 nibbles of 4 pages. The page number (PG) register of RAM defined by the MPG instruction, and its initial value is 0. Because the memory space is shared with the memory registers (address=0x00~0x07), the address for RAM is 0x08~0x3F.

In addition to the immediate addressing mode, the indexed addressing mode is also supported. The page and address of the indexed RAM should be stored into RPT1 and RPT0 first, and users can read from or write in the XMD memory register to realize the indexed ROM access.

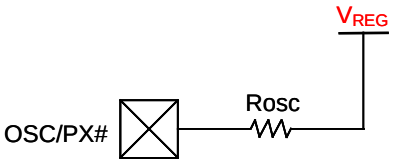
6. Clock Generator

The clock generator is a Ring oscillator, and users can select the internal resistor (INT-R) or the external resistor (EXT-R). A precise INT-R oscillator is provided, and its accuracy is up to ±1%.

For NY5P025A ~ 5P085A bodies if OSC/PD2 pad is optioned as PD2 I/O function, or for NY5P185A ~ 5P345A bodies if OSC/PE3 pad is optioned as PE3 I/O function or for NY5P520A ~NY5P720A bodies if OSC/PF3 is optioned as PF3 I/O function, there is only INT-R, and EXT-R is disabled. When this pad is optioned as OSC function oppositely, INT-R or EXT-R can be determined by the configurations below. And the OSC pad must be connected to V_{REG} rather than V_{DD} when using EXT-R.



INT-R Oscillator Connection



EXT-R Oscillator Connection

7. IO PORTS

There are most 24 I/O ports, designated as PAx through PFx, and x=0~3. All the I/O ports can be configured as input, output, or IO port (bi-direction). For the input port, we provide an internal pull-high register option for convenience. For the output port, users can also option its initial value as low or high according to your application circuit. Besides, users can also enable the large current option for each output port to get a larger sink current. The bi-direction IO port can be an input or output by its register value, and users can option the bi-direction IO with a pull-high resister or without a pull-high resister (Open-Drain). When the register equals 0, it is an output and can only output zero. When the register equals 1, it is a weak pull-high or floating (Open-Drain) so that it also can be considered as an input port with/without a pull-high resistor. Users also can enable the large sink current option of an IO port.

The PX0 port means the PA0, PB0, PC0, PD0, PE0 or PF0 port can also be optioned as an external reset pin or an infrared (IR) output pin. A reset port can possess a pull-high resister or not, and an IR port can be initial low or high and also large sink current or not.

The pull-high resister of all the I/O ports has two kinds of option: weak and strong. The weak one is about 850KΩ @3V for normal application and the strong one is about 480KΩ @3V usually for key matrix function. When users configure the weak or strong pull-high resister, the pull-high resisters of all I/O ports are set as the option value.

For NY5P025A ~ NY5P085A bodies, PD2 pad is shared with external OSC pad. When users enable external OSC function, PD2 function will be disabled. For NY5P185A ~ NY5P345A bodies, PE3 pad is shared with external OSC pad. When users enable external OSC function, PE3 function will be disabled. For NY5P520A ~ NY5P720A bodies, PF3 pad is shared with external OSC pad. When users enable external OSC function, PF3 function will be disabled.

8. AUDIO SYNTHESIZER

There are 1-ch voice and 2-ch or 4-ch speech/Midi, and all modes are auto-played back by hardware. Different channel mode possesses different hardware structure. It provides a hardware mixer to mix the channel data. The mixer contains a mixer control register MIX. 1-ch ~ 4-ch voice and/or Midi are all configurable by programming the MIX Two audio output stages: DAC and PWM are supported.

8.1 Voice

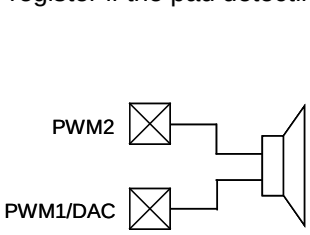
A voice channel includes a PFLG, a VPR, a voice decoder, a QIO control code generator and an 8-bit sample rate timer (TM) whose timer clock source (TCS) is fixed to 1MHz. It supports PCM and encoded ADPCM speech data.

8.2 Midi

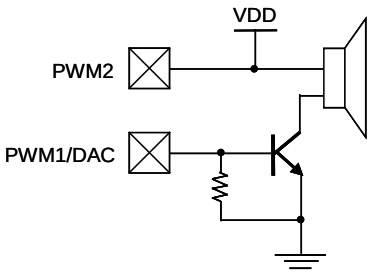
A Midi channel includes a PFLG, a VPR, a TM, an ENV, a timbre skipper and a multiplier, which multiplies the Midi data and the envelope value held by the ENV. The timbre skipper is used to fulfill the higher octave pitch playing. The hardware multiplier is dedicated to the Midi channel, and users can't operate it by any instruction.

8.3 Audio Output

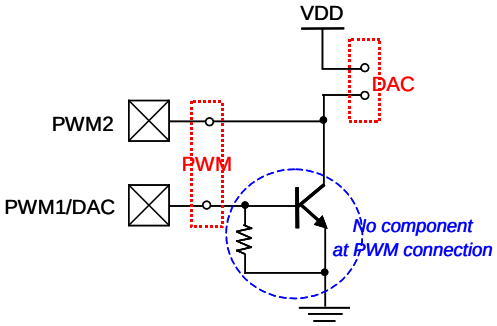
By setting the AUD register, PWM or DAC can be easily chosen as the audio output stage. Besides, it provides a pad detecting mechanism. The pad detecting mechanism detects the PWM2 pad during the reset initialization period, and sets the initial value of the audio output register as PWM if the PWM2 connection is floating, or sets the initial value of the audio output register as DAC if the PWM2 connection is high. In conclusion, connect the speaker to PWM1 and PWM2 only if using PWM, otherwise connect PWM2 to VDD if using DAC. Since the mechanism sets only the initial value of AUD, don't change the value of the AUD register if the pad detecting mechanism is adopted.



PWM Output Connection



DAC Output Connection



PWM/DAC Connection Together

When using the PWM output, we provide an option of normal PWM current or large PWM current for different customer demand. The large PWM consumes more current and makes sound louder.

8.4 Volume Control

Both PWM and DAC support 16 steps hardware volume control by the VOL register.

9. ELECTRICAL CHARACTERISTICS

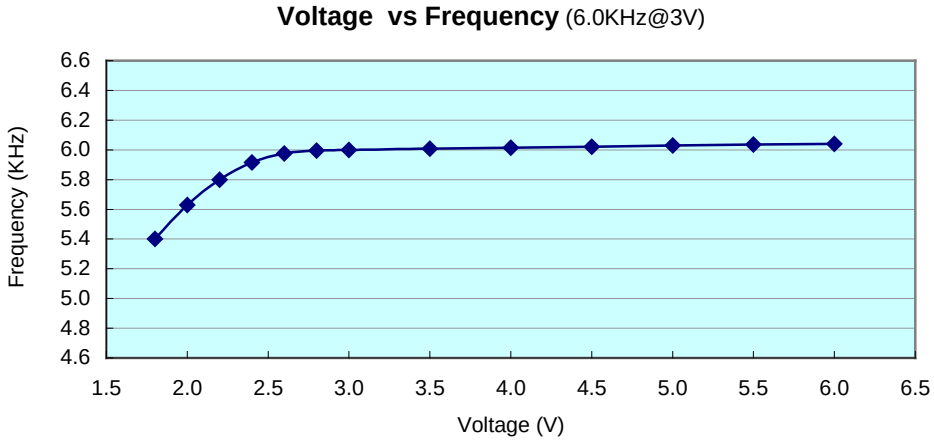
9.1 Absolute Maximum Rating

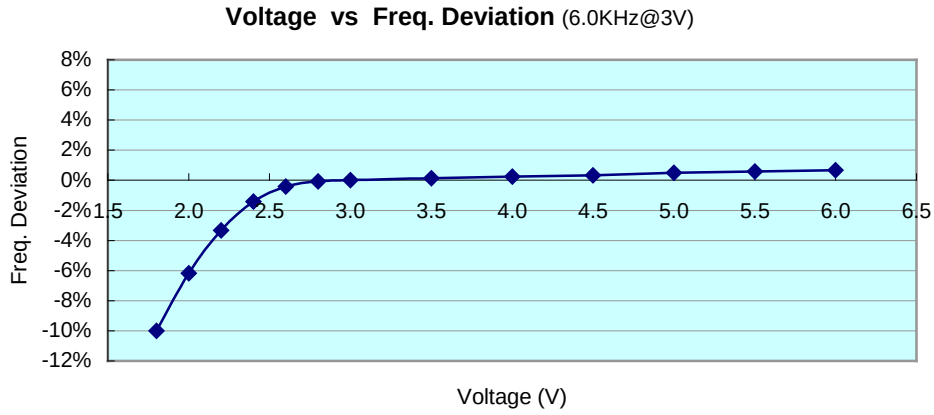
Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

9.2 DC Characteristics

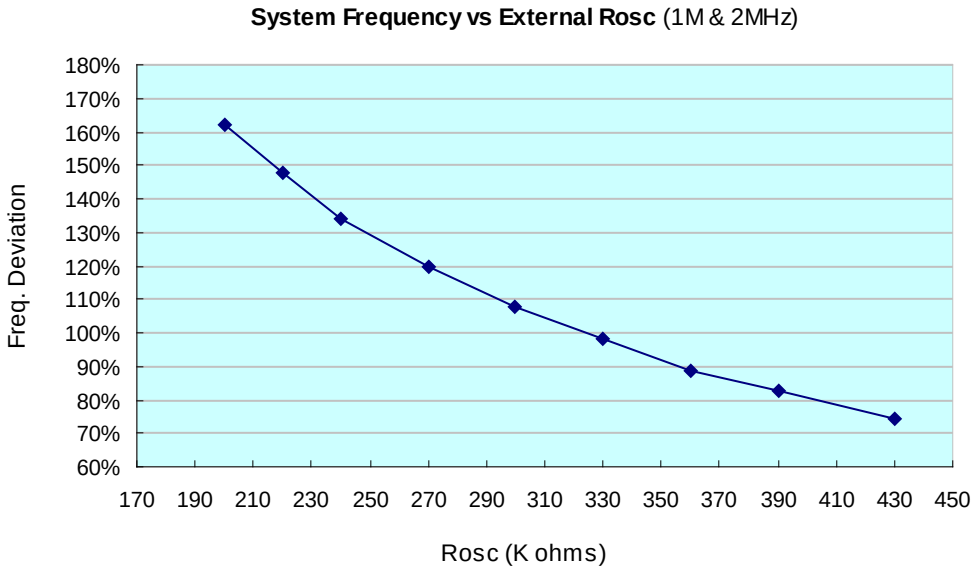
Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	1MHz & 2MHz
Isb	Supply current	Halt mode	3			1	uA	Sleep, no loading
			4.5			1		
Isl		Slow mode	3		150		uA	1ms interrupt, no load
			4.5		350			
Iop		Operating mode	3		2		mA	1MHz, no loading
			4.5		2.4			
			3		2.5		mA	2MHz, no loading
			4.5		2.8			
Iil	Input current (Internal pull-high)	Weak (850k ohms)	3		-3.5		uA	Vil=0v
			4.5		-10			
		Strong (480k ohms)	3		-7		uA	
			4.5		-20			
Ioh	Output high current		3		-10		mA	Voh=1.0V
			4.5		-22			Voh=2.2V
Iol	Output low current (Normal current)		3		10		mA	Vol=2.0V
			4.5		20			Vol=2.5V
	Output low current (Large current)		3		20		mA	Vol=2.0V
			4.5		40			Vol=2.5V
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
	PWM output current (Large)		3		70		mA	Load=8 ohms
			4.5		117			
I_{DAC}	DAC output current		3	-0.36 ~ -4.20			mA	Half scale
			4.5	-0.47 ~ -4.85				
△F/F	Frequency deviation by voltage drop		3		1.5		%	Fosc(3.0v)-Fosc(2.4v) / Fosc(3v)
			4.5		0.5			Fosc(4.5v)-Fosc(3.0v) / Fosc(4.5v)
△F/F	Frequency lot deviation		3	-1		1	%	Fmax(3.0v)-Fmin(3.0v) / Fmax(3.0v)
Fosc	Oscillation Frequency		-	0.90	1	1.05	MHz	VDD=2.0~5.5V
				1.80	2	2.10		

9.3 Voltage vs. Frequency





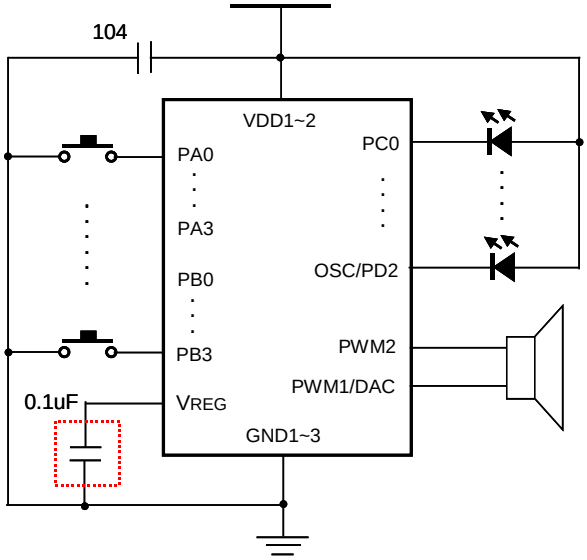
9.4 System Frequency v.s. External Rosc



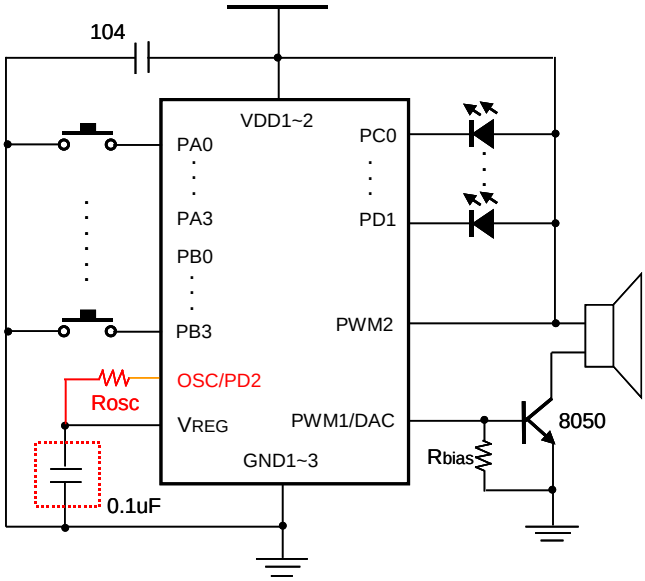
10. APPLICATION

10.1 NY5P025A, NY5P055A, NY5P085A

(1) INT-R, PWM *(OSC/PD2 is optioned as PD2 pad)*

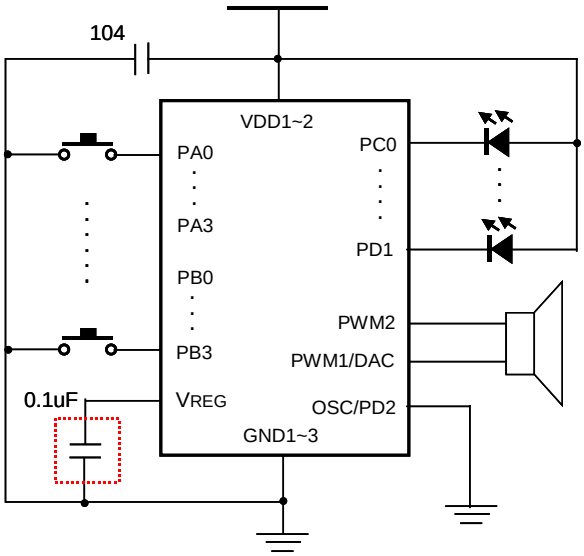


(2) EXT-R, DAC *(OSC/PD2 is optioned as OSC pad)*



Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

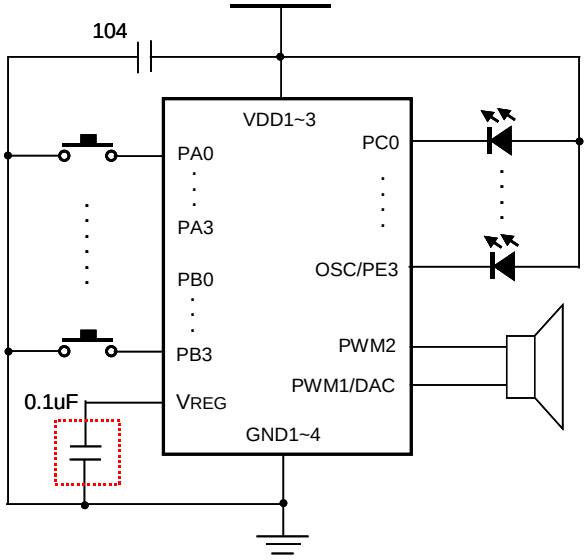
(3) INT-R, PWM *(OSC/PD2 is optioned as OSC pad)*



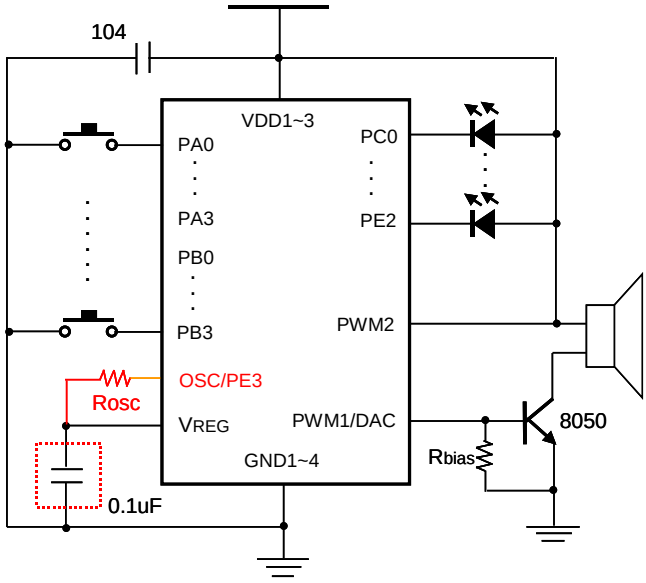
Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

10.2 NY5P185A, NY5P345A

(1) INT-R, PWM ***(OSC/PE3 is optioned as PE3 pad)***

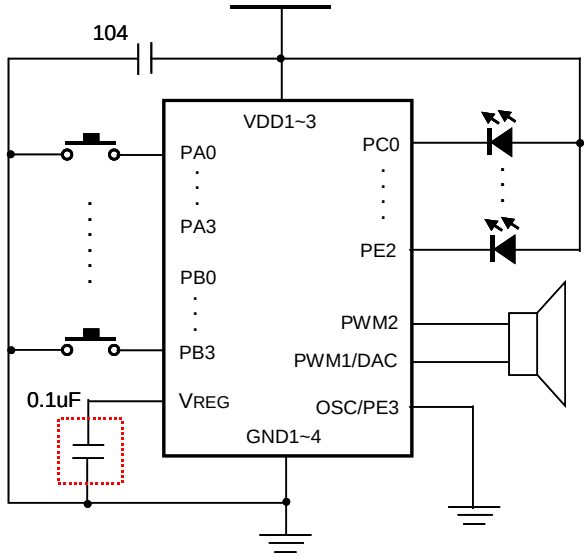


(2) EXT-R, DAC ***(OSC/PE3 is optioned as OSC pad)***



Note: While using external OSC, the OSC pad must be connected to VREG rather than VDD.

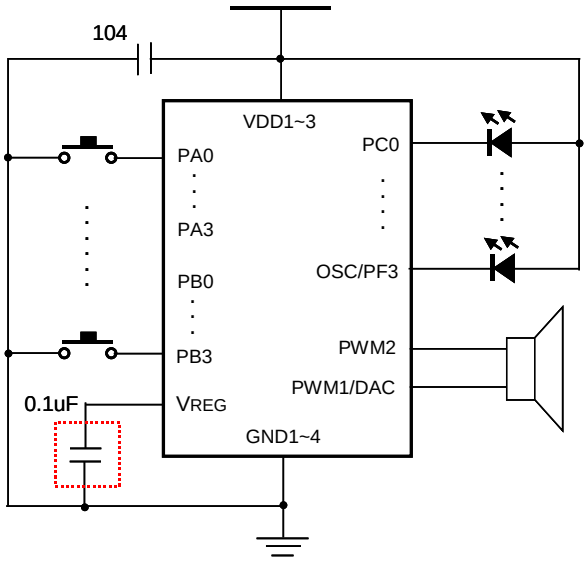
(3) INT-R, PWM ***(OSC/PE3 is optioned as OSC pad)***



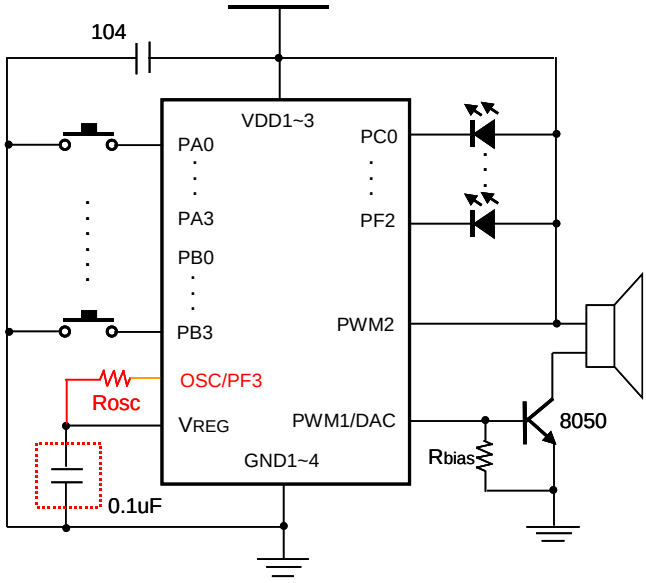
Note: At high voltage of 4.5V or higher voltage, VREG maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, VREG don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

10.3 NY5P520A, NY5P720A

(1) INT-R, PWM ***(OSC/PE3 is optioned as PE3 pad)***

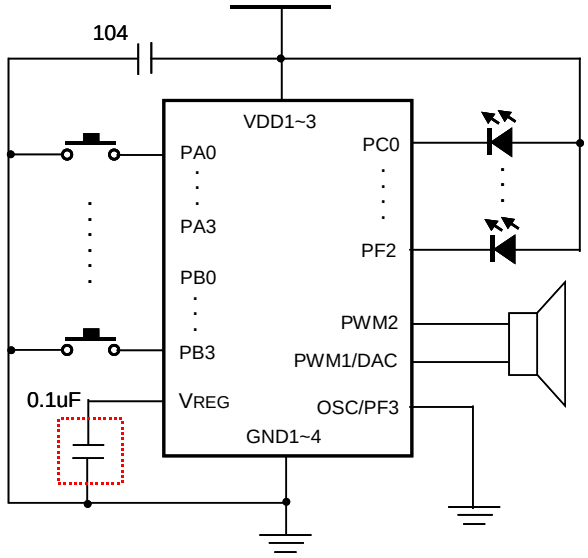


(2) EXT-R, DAC ***(OSC/PE3 is optioned as OSC pad)***



Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

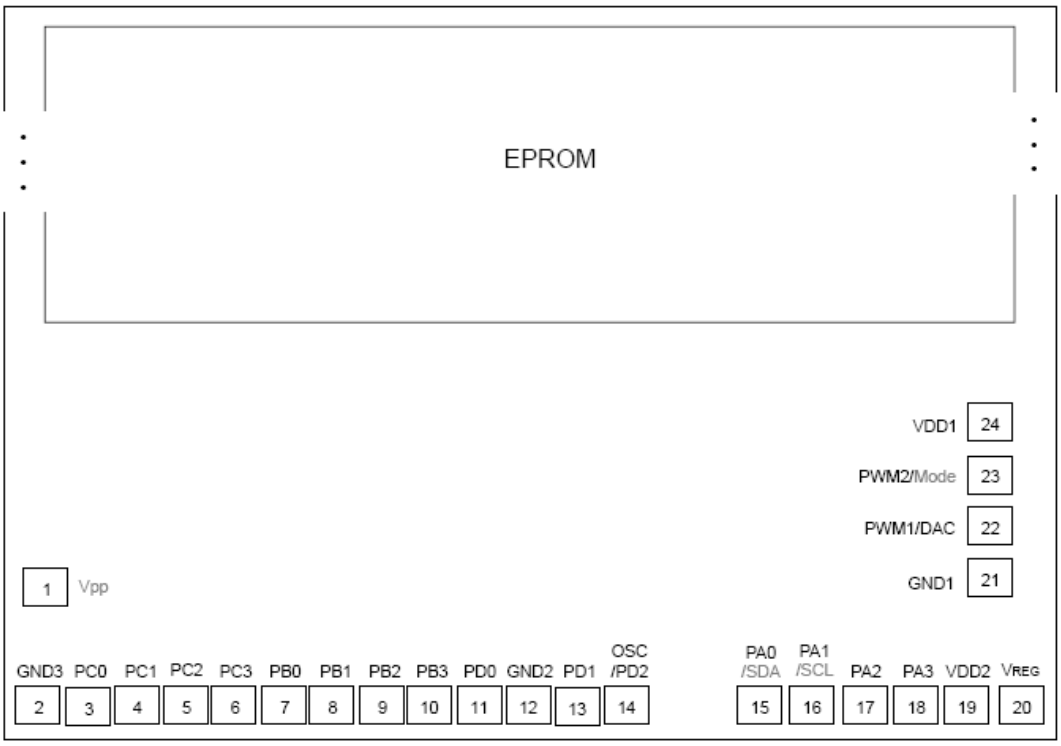
(3) INT-R, PWM ***(OSC/PE3 is optioned as OSC pad)***



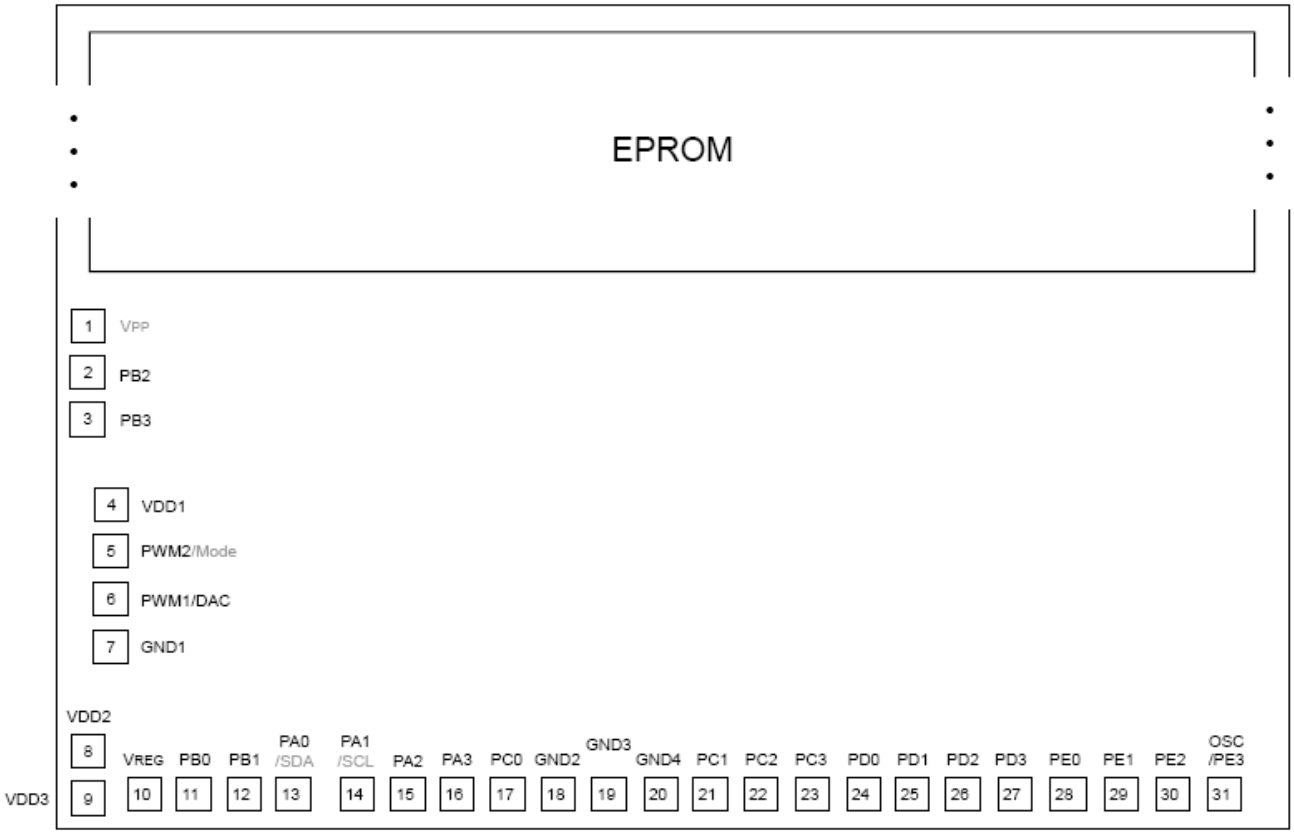
Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

11. DIE PAD DIAGRAM

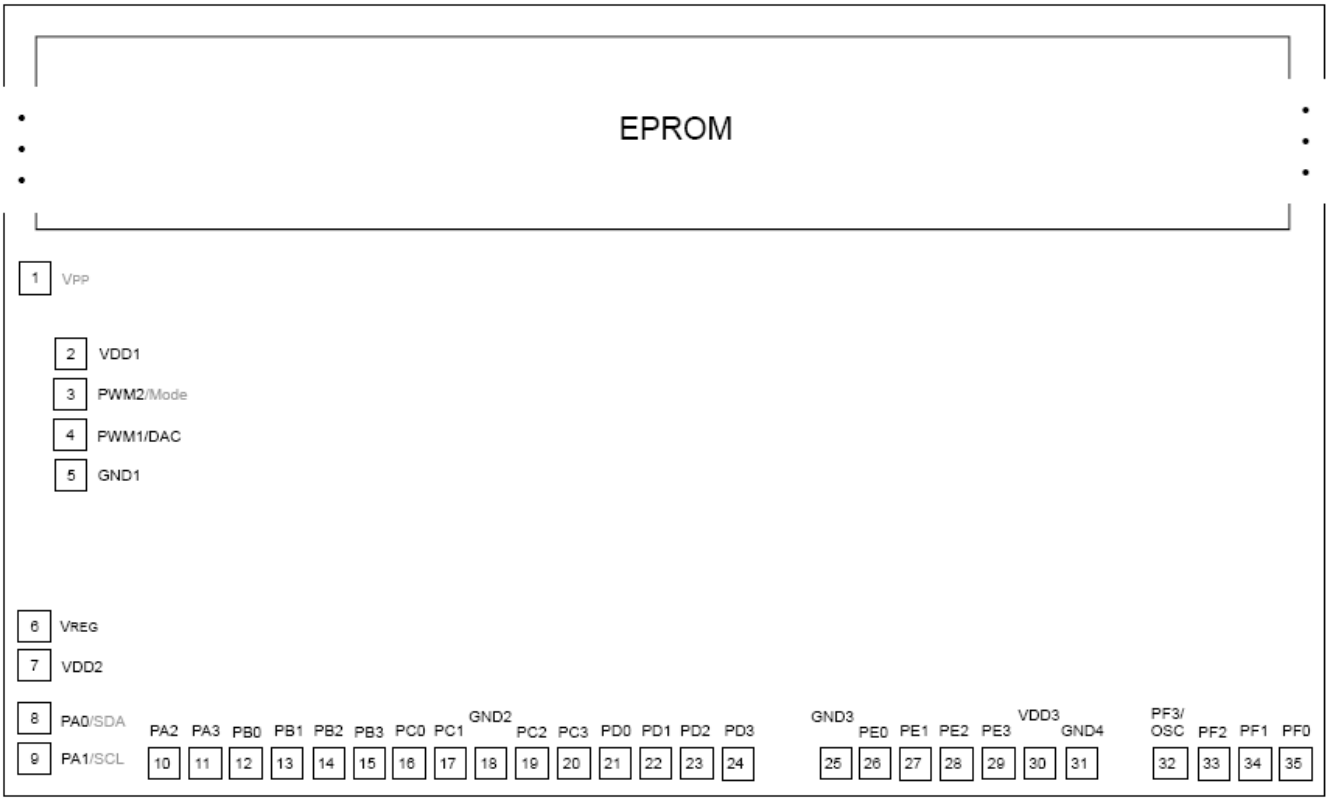
11.1 NY5P025A, NY5P055A, NY5P085A



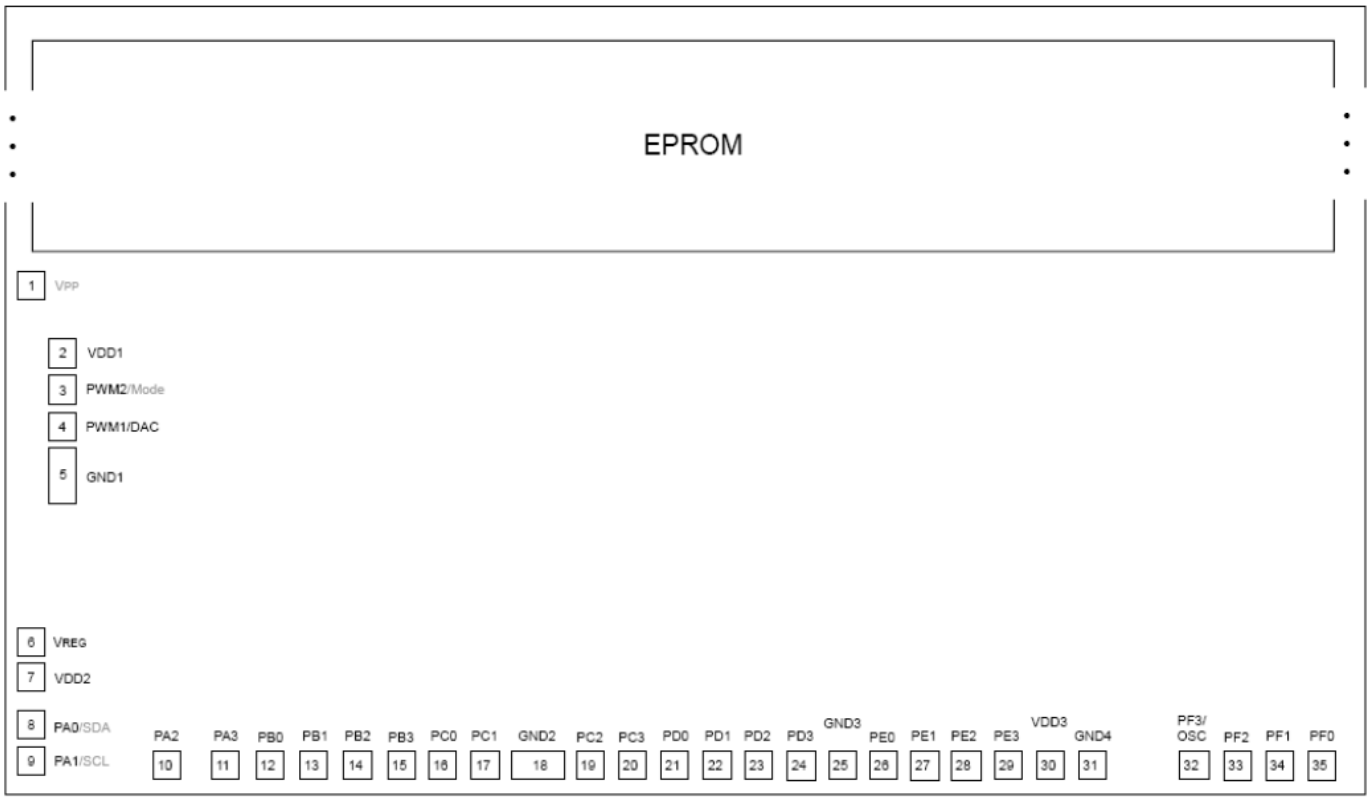
11.2 NY5P185A, NY5P345A



11.3 NY5P520A

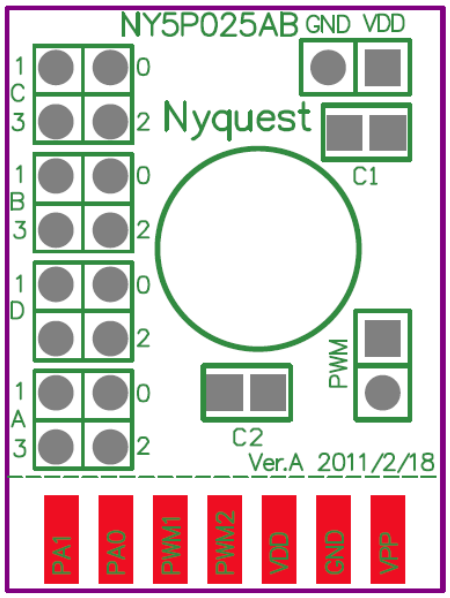


11.4 NY5P720A

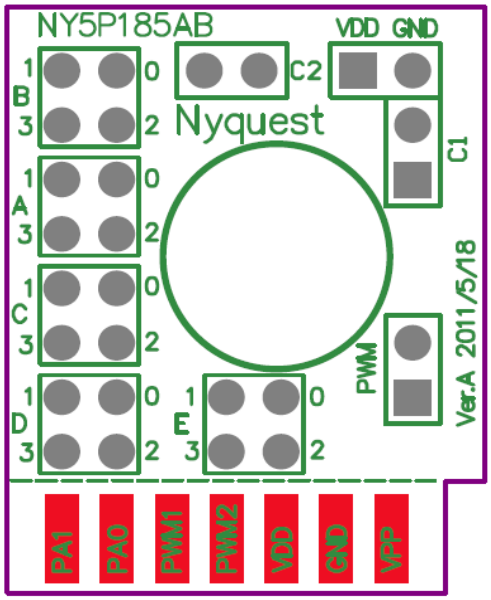


12. COB PIN ASSIGNMENT

NY5P025AB, NY5P055AB, NY5P085AB ***(15 I/O)***

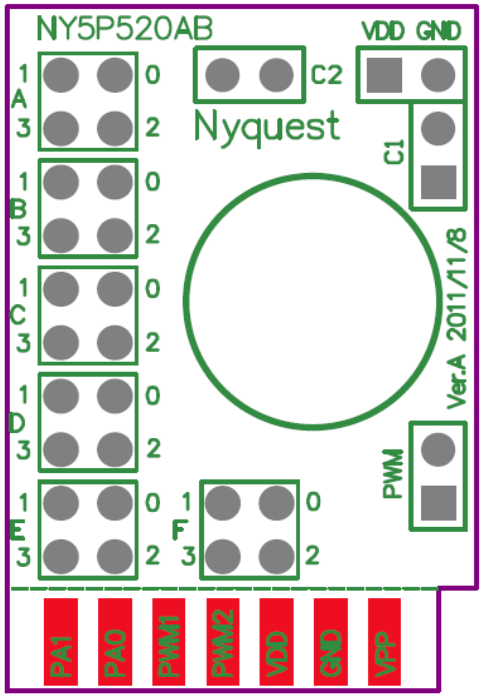


NY5P185AB, NY5P345AB ***(20 I/O)***



Note: C1 is VDD power cap, C2 is Vreg cap.

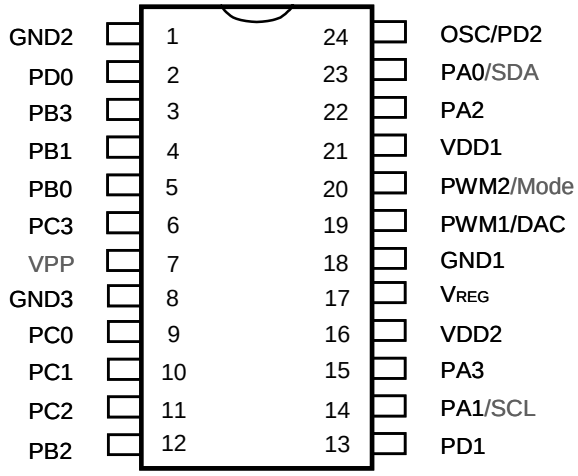
NY5P520AB, NY5P720AB ***(24 I/O)***



Note: C1 is VDD power cap, C2 is Vreg cap.

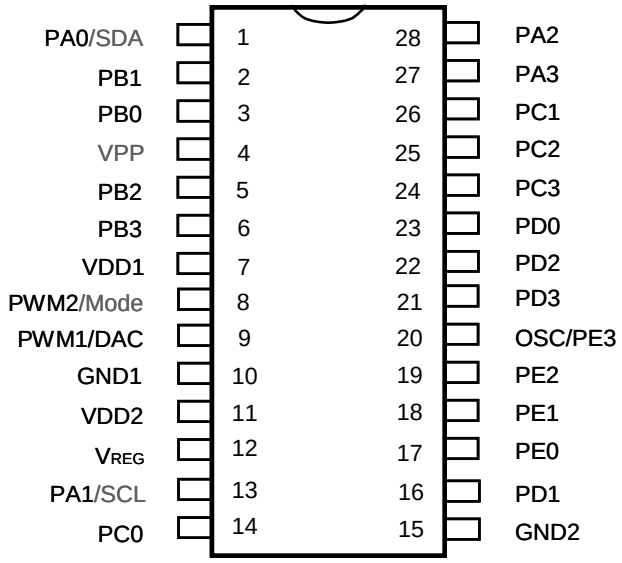
13. PACKAGE PIN ASSIGNMENT

24-pin SOP (300mil)



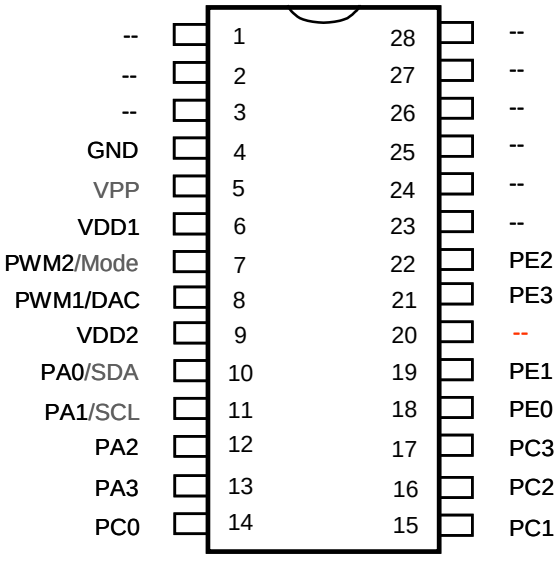
NY5P025AS24
NY5P055AS24
NY5P085AS24

28-pin SOP (300mil)



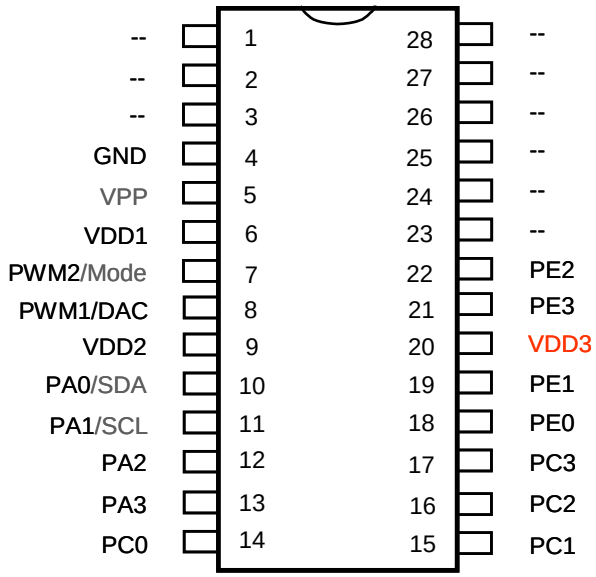
NY5P185AS28

28-pin SOP (300mil)

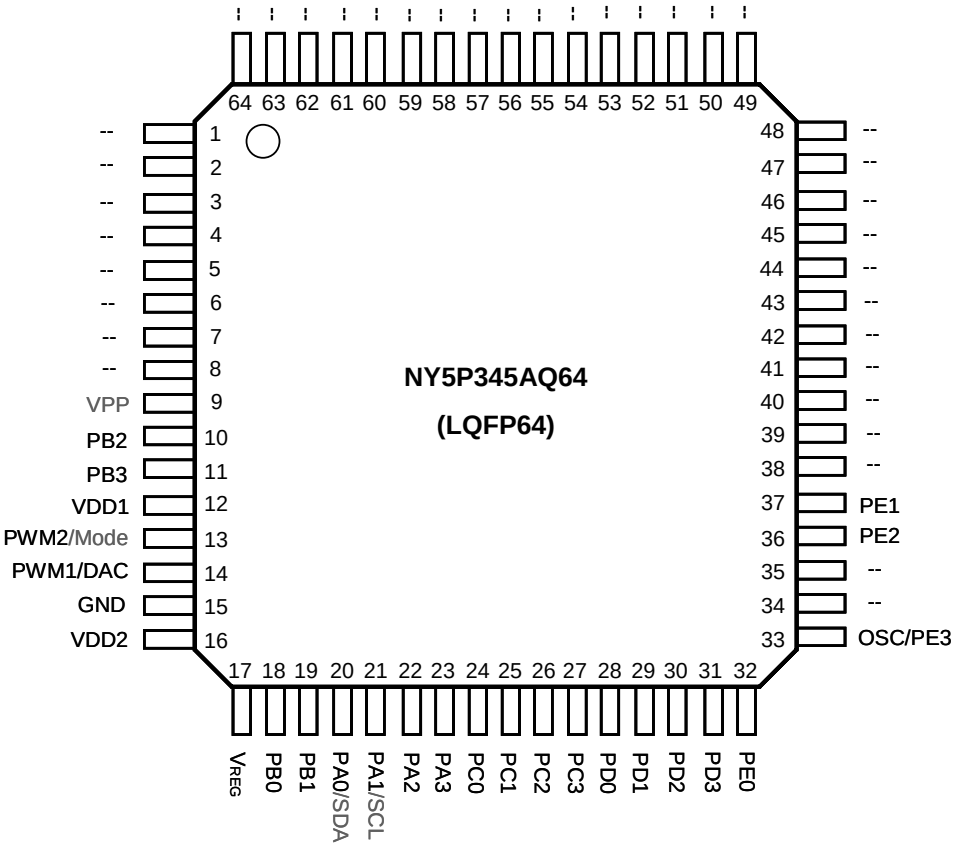


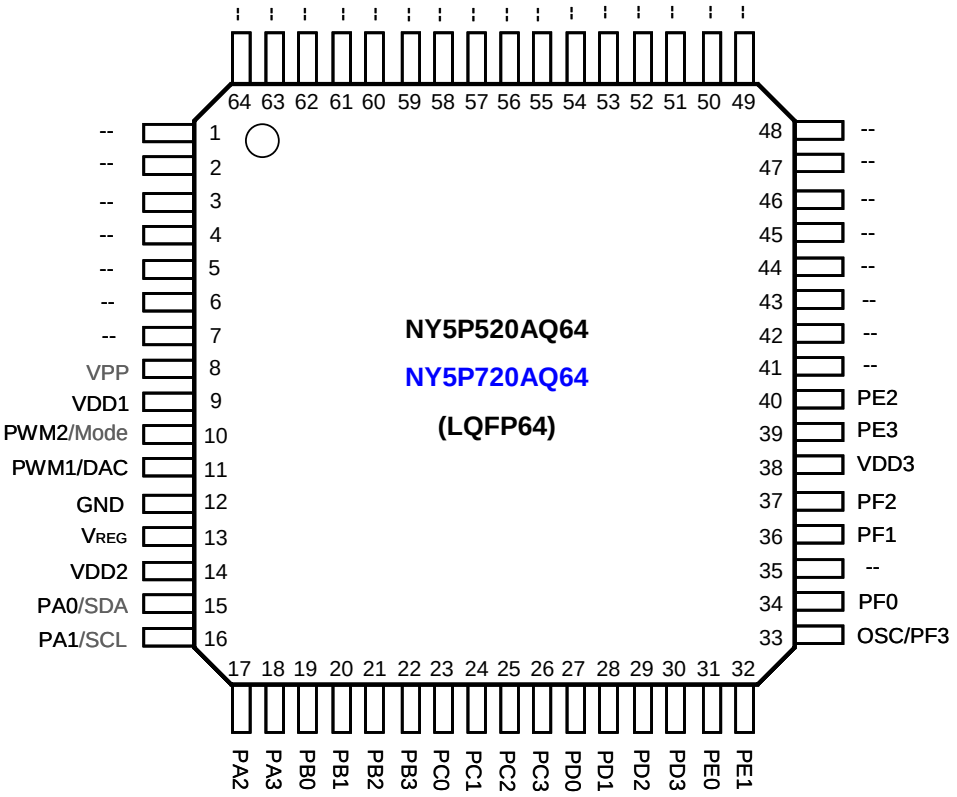
NY5P345AS28

28-pin SOP (300mil)



NY5P520AS28

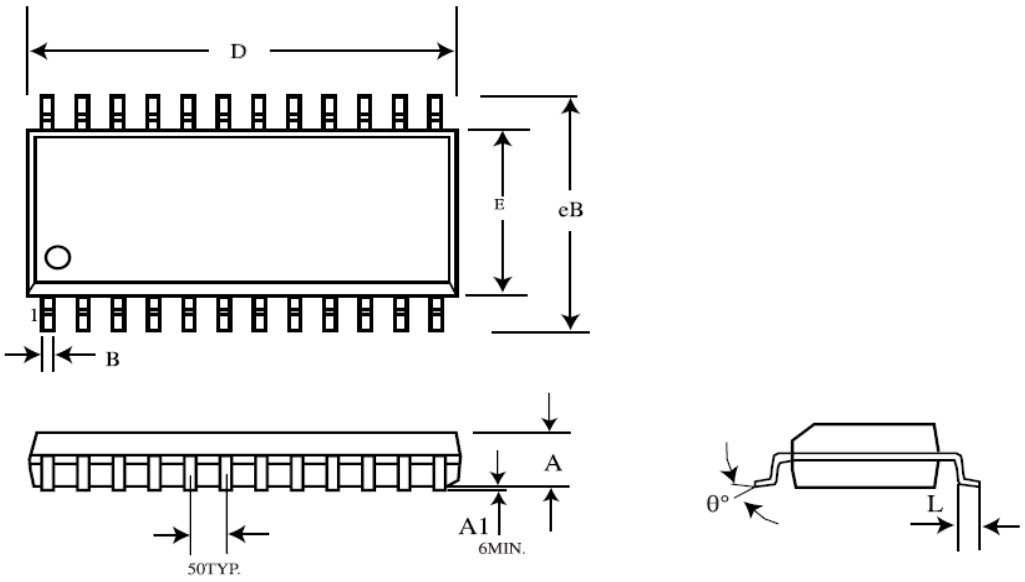




" -- " means "Not Connection" (N/C).

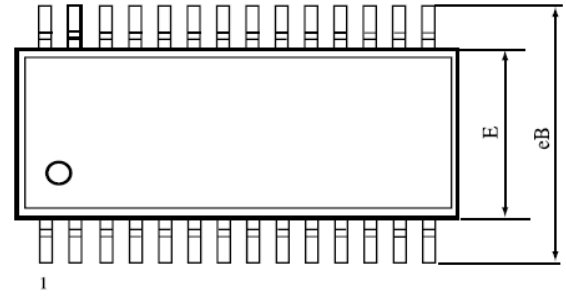
14. PACKAGE DIMENSION

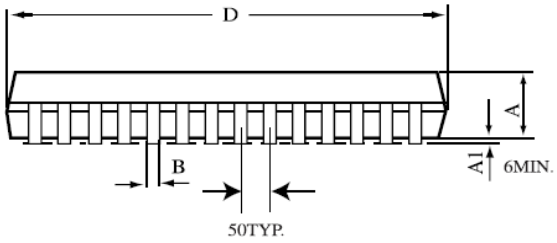
24-Pin Plastic SOP (300 mil)

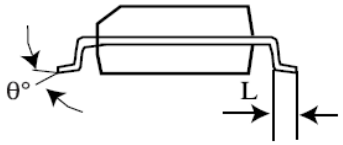


Sym.	Dimension in mils			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	98	100	102	2.489	2.540	2.591
A1	6	- - -	- - -	0.152	- - -	- - -
B	12	16	20	0.305	0.406	0.508
D	606	608	610	15.392	15.443	15.494
E	298	300	302	7.569	7.620	7.671
eB	406	410	414	10.312	10.414	10.516
L	25	- - -	- - -	0.635	- - -	- - -
θ°	0°	4°	8°	0°	4°	8°

28-Pin Plastic SOP (300 mil)

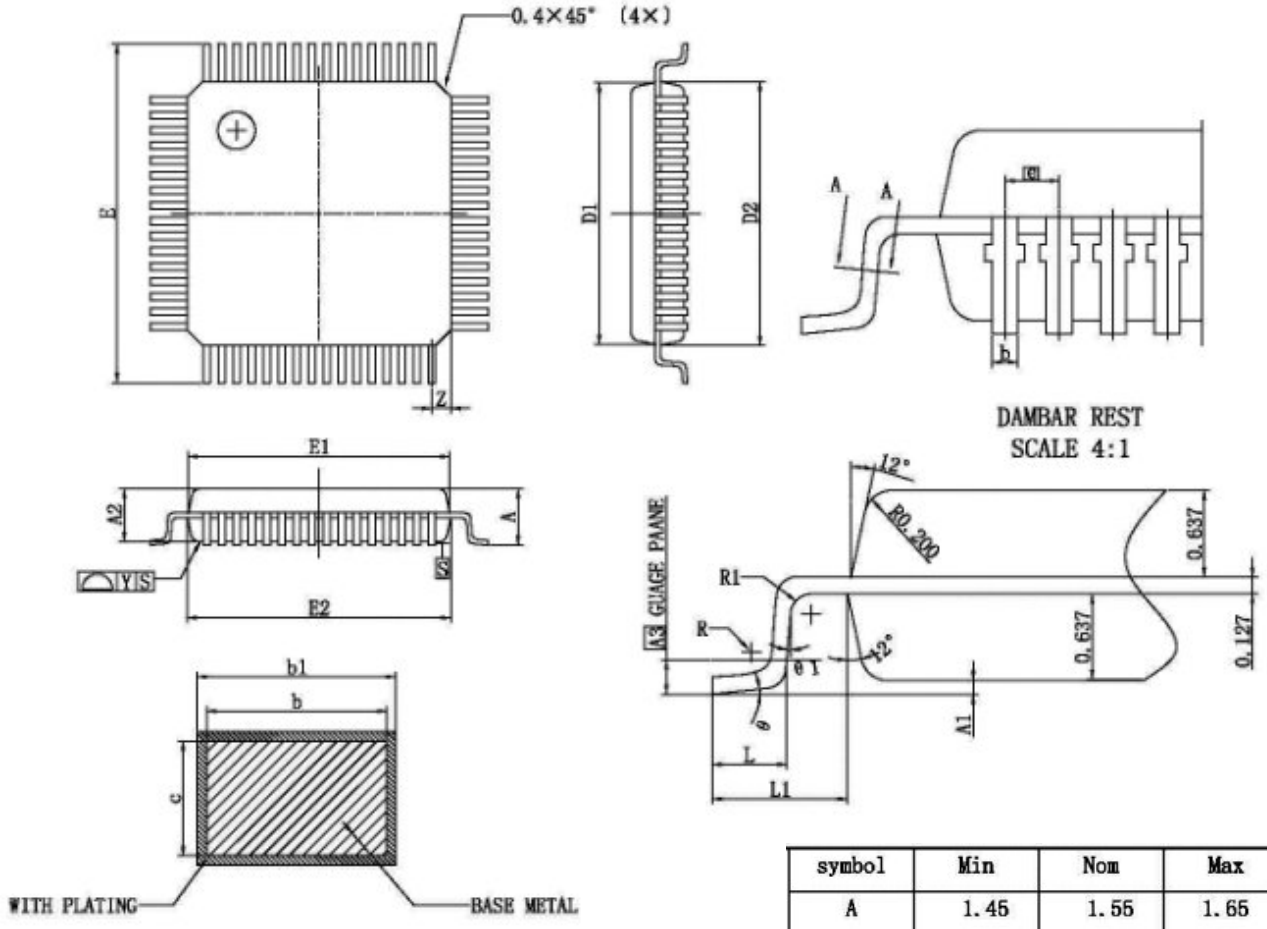






Sym.	Dimension in mils			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	90	92	94	2.286	2.337	2.388
A1	6	- - -	- - -	0.152	- - -	- - -
B	12	16	20	0.305	0.406	0.508
D	703	705	707	17.856	17.907	17.958
E	293	295	297	7.442	7.493	7.544
eB	406	410	414	10.312	10.414	10.516
L	25	- - -	- - -	0.635	- - -	- - -
θ°	0°	4°	8°	0°	4°	8°

64-Pin LQFP (7mm x 7mm)



SECTION A-A

symbol	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.01	—	0.21
A2	1.3	1.4	1.5
A3	—	0.254	
b	0.13	0.18	0.23
b1	0.14	0.20	0.26
c	—	0.127	—
D1	6.85	6.95	7.05
D2	6.9	7.00	7.10
E	8.8	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	—	0.4	—
L	0.43	—	0.71
L1	0.90	1.0	1.10
R	0.1	—	0.25
R1	0.1	—	—
θ	0	—	10°
θ1	0	—	—
y	—	—	0.1
Z	—	0.5	—

NOTE:
1. All dimensions are in mm.
2. Dim D1/D2 & E1/E2 does not include plastic flash.
Flash: Plastic residual around body edge after dejunk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.005~0.015mm.

15. ORDERING INFORMATION

P/N	Shipping Type	Remarks
NY5P025A	Die	Empty ROM data
NY5P025A-xxxx *1	Die	Programmed ROM data
NY5P025AW-xxxx *1	Wafer	Programmed ROM data
NY5P025AB	COB	20.3mm x 22.1mm (20.3mm x 27.3mm w/ V-Cut)
NY5P025AS24	SOP-24	Width 300 mil
NY5P055A	Die	Empty ROM data
NY5P055A-xxxx *1	Die	Programmed ROM data
NY5P055AW-xxxx *1	Wafer	Programmed ROM data
NY5P055AB	COB	20.3mm x 22.1mm (20.3mm x 27.3mm w/ V-Cut)
NY5P055AS24	SOP-24	Width 300 mil
NY5P085A	Die	Empty ROM data
NY5P085A-xxxx *1	Die	Programmed ROM data
NY5P085AW-xxxx *1	Wafer	Programmed ROM data
NY5P085AB	COB	20.3mm x 22.1mm (20.3mm x 27.3mm w/ V-Cut)
NY5P085AS24	SOP-24	Width 300 mil
NY5P185A	Die	Empty ROM data
NY5P185A-xxxx *1	Die	Programmed ROM data
NY5P185AW-xxxx *1	Wafer	Programmed ROM data
NY5P185AB	COB	22.1mm x 22.1mm (22.1mm x 27.3mm w/ V-Cut)
NY5P185AS28	SOP-28	Width 300 mil
NY5P345A	Die	Empty ROM data
NY5P345A-xxxx *1	Die	Programmed ROM data
NY5P345AW-xxxx *1	Wafer	Programmed ROM data
NY5P345AB	COB	22.1mm x 22.1mm (22.1mm x 27.3mm w/ V-Cut)
NY5P345AS28	SOP-28	Width 300 mil
NY5P345AQ64	LQFP-64	Quad 7mm x 7mm
NY5P520A	Die	Empty ROM data
NY5P520A-xxxx *1	Die	Programmed ROM data
NY5P520AW-xxxx *1	Wafer	Programmed ROM data
NY5P520AB	COB	22.1mm x 27.6mm (22.1mm x 32.5mm w/ V-Cut)
NY5P520AS28	SOP-28	Width 300 mil
NY5P520AQ64	LQFP-64	Quad 7mm x 7mm
NY5P720A	Die	Empty ROM data
NY5P720A-xxxx *1	Die	Programmed ROM data
NY5P720AW-xxxx *1	Wafer	Programmed ROM data
NY5P720AB	COB	22.1mm x 27.6mm (22.1mm x 32.5mm w/ V-Cut)
NY5P720AQ64	LQFP-64	Quad 7mm x 7mm

**1 "xxxx": Code number*